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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,795	10/16/2003	Joseph John Sumakeris	5308-286	7928
20792	7590	03/25/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627			NGUYEN, CUONG QUANG	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,795	SUMAKERIS ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 and 31-45 is/are pending in the application.
- 4a) Of the above claim(s) 10-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-7,9,31,32,35,37-40,42,44 and 45 is/are rejected.
- 7) ☒ Claim(s) 3,8,33,36 and 41 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>01-24-05, 0830-04.</u> | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Species I (Fig.1), claims 1-9, 11-16, 31-32 and 44-45 is acknowledged. However, the limitation (diode) in claims 11-16 does not belong to elected species, it belongs to Fig.3. So, claims 11-16 also has been withdrawn from consideration.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4, 5, 9, 31, 32, 37, 38, 42, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al. (WO 02/299900 A2) in view of Zommer (US 6,162,665).

Regarding claims 1, 4, 5, 9, 38, 42, 44, 45, Ryu et al. discloses a method of forming a silicon carbide MOSFET comprising the step of: forming a drift layer (12) consisting of a substrate (page 15, lines 2-5), and therefore implicitly boule-grown in the case of Sic substrates, this drift layer having a net carrier concentration down to 10^4 Cm^3 and therefore less than $2 \times 10^5 \text{ Cm}^3$. The method discloses further the steps of forming a p-

type Sic base region, an n-type Sic source region on the drift layer and a gate electrode on the p-type base region. See Fig.6, 8A-H, 9A-J.

Ryu et al. does not explicitly teach that the device has a 10 kV or higher high blocking voltage rating as claimed.

Zommer teaches that the thickness and dopants in the substrate and epitaxial layer are tailor to create the desired high voltage characteristics. Zommer also suggested that the thickness between about 200 microns to 500 microns would be preferred.

It would have been obvious to one of ordinary skill in the art to form the drift layer having thickness as suggested by Zommer in order to obtain a high voltage characteristics such as the device has a 10 kV or higher high blocking voltage rating as claimed. Furthermore, the blocking voltage rating of such a device is not specified in the Ryu, but it is obvious to the person skilled in the art, that thickness and doping of the substrate-drift layer can always be adjusted to reach also high blocking voltage in the range of 10 KV or higher, if the circumstances (i.e. the applications) require it.

Regarding claim 31, Ryu discloses also the formation of a n-type silicon carbide epilayer (124) on the drift-substrate layer (12),. See Fig. 9C and associated text.

Regarding claims 32, 37, Ryu teaches that the drift-substrate layer can be used for a Sic JFET.

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Claims 2, 6, 7, 35, 39, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al. in view of Zommer and further in view of Baranov et al. (EPR study of shallow and deep phosphorous centers in 6H-SiC).

Regarding claims 2, 6, 35, 39, the combination of Ryu et al. and Zommer does not explicitly teach that the method forming a silicon carbide drift layer comprises annealing a boule-grown silicon carbide wafer at a sufficient temperature to reduce a trap density therein.

Baranov teaches that annealing is a standard procedure after the NTD process to activate the phosphorous dopant and to anneal the defects in the SiC material, thus reducing the trap density in the wafer and increasing the minority carrier lifetime (see INTRODUCTION and first par of EXPERIMENTAL DETAILS).

It would have been obvious to one of ordinary skill in the art to form the Ryu et al.'s device including the step of annealing a boule-grown silicon carbide wafer at a sufficient temperature to reduce a trap density therein as taught by Baranov in order to activate the phosphorous dopant and to anneal the defects in the SiC material, thus reducing the trap density in the wafer and increasing the minority carrier lifetime (see INTRODUCTION and first par of EXPERIMENTAL DETAILS).

Regarding claims 7, 40, it is noted that planarizing a SiC wafer/substrate is a common practice before any processing step taking place on it, furthermore thinning the

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substrate to tailor the blocking voltage of this kind of devices is also a well known practice, see for example Zommer: col. 2, lines 8-23 and col. 4, lines 30-65).

So, it would have been obvious to one of ordinary skill in the art to thinner the drift layer by conventional method of planarizing to obtain a specific thickness.

Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al. in view of Baranov et al. and Heissenstein (Characterization of phosphorous doped n-type 6H-silicon carbide epitaxial layers produced by nuclear transmutation doping).

Baranov does not teach that annealing is a standard procedure after the NTD process to activate

the phosphorous dopant and to anneal the defects in the Sic material, thus

reducing the trap density in the wafer and increasing the minority carrier lifetime

(see for example also D5: INTRODUCTION and first par. of EXPERIMENTAL DETAILS).

Allowable Subject Matter

3. Claims 3, 8, 33, 34, 36, and 41 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

5. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

7. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

3/16/05

